

Abstract of the Disclosure

A method of forming an integrated circuit dual gate structure using only one mask is disclosed. In one embodiment, a substrate is prepared for the fabrication of a dual gate structure, a first gate structure having an NWELL is formed without using a
5 mask, and a second gate structure having a PWELL is formed using only one mask. In an alternate embodiment, a substrate is prepared for the fabrication of a dual gate structure, a first gate structure having a PWELL is formed without using a mask, and a second gate structure having an NWELL is formed using only one mask.

20010213-0001

"Express Mail" mailing label number: EL709303714US
Date of Deposit: February 13, 2001

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